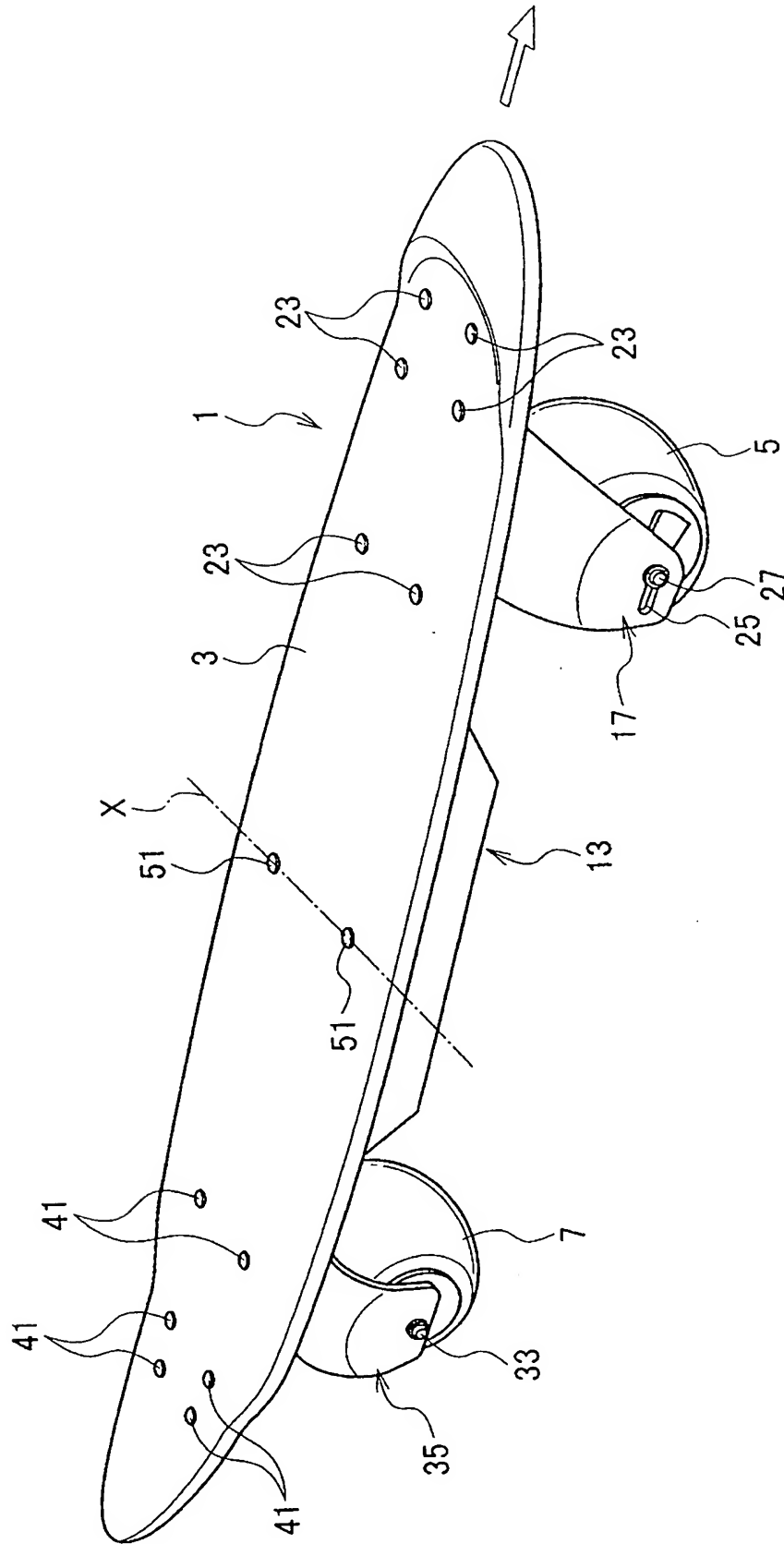


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FIG. 1



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FIG. 2

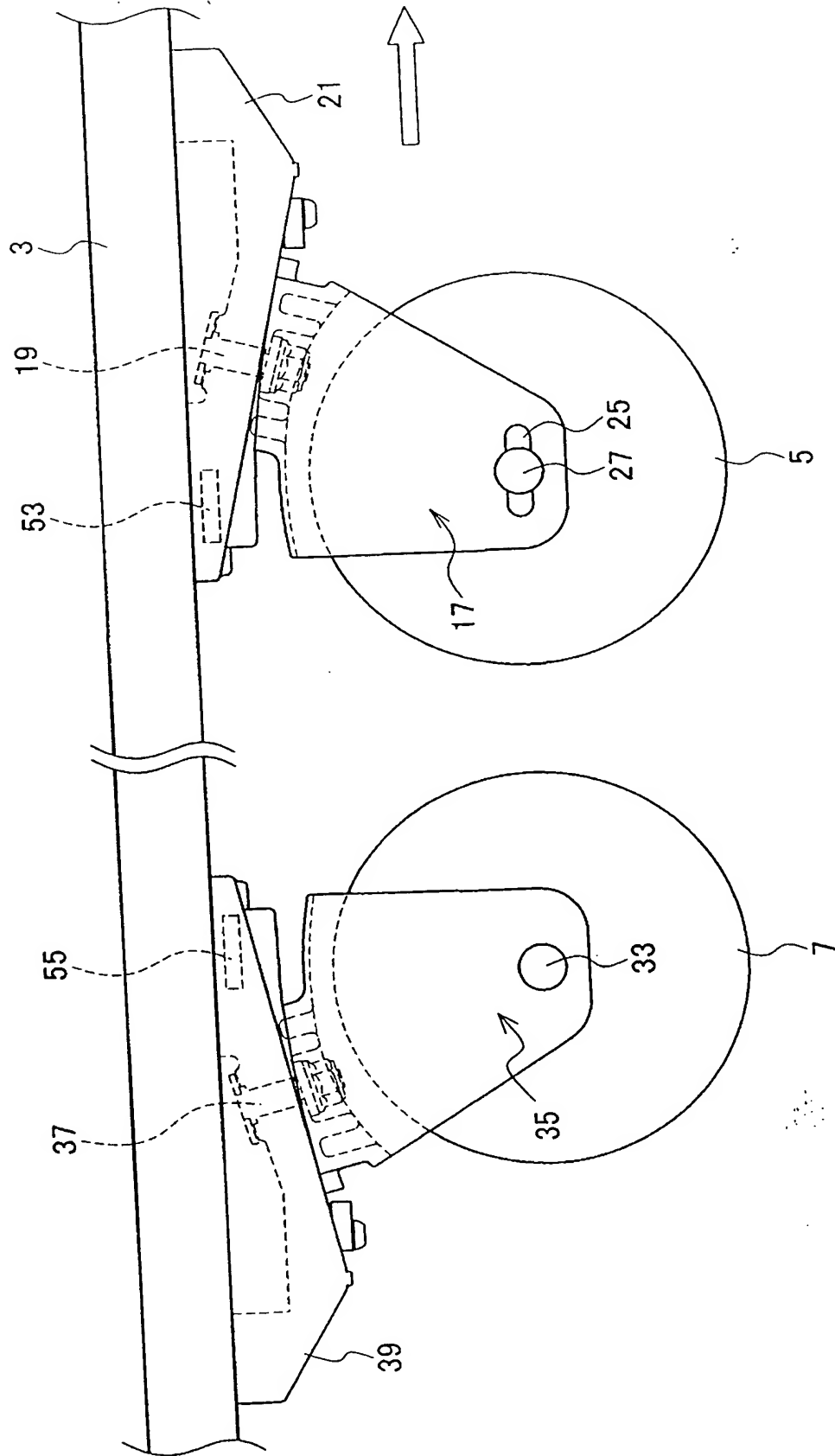
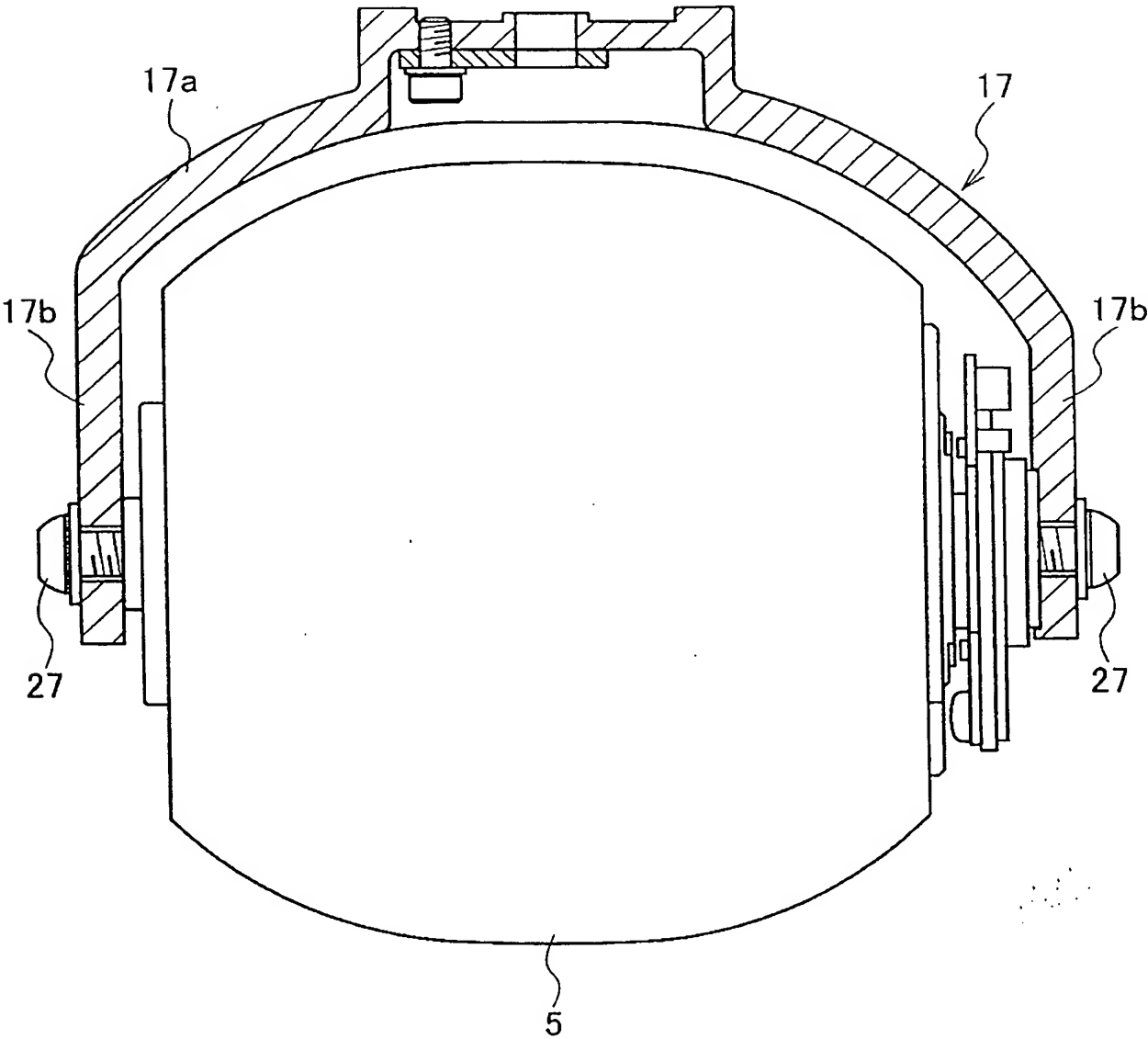
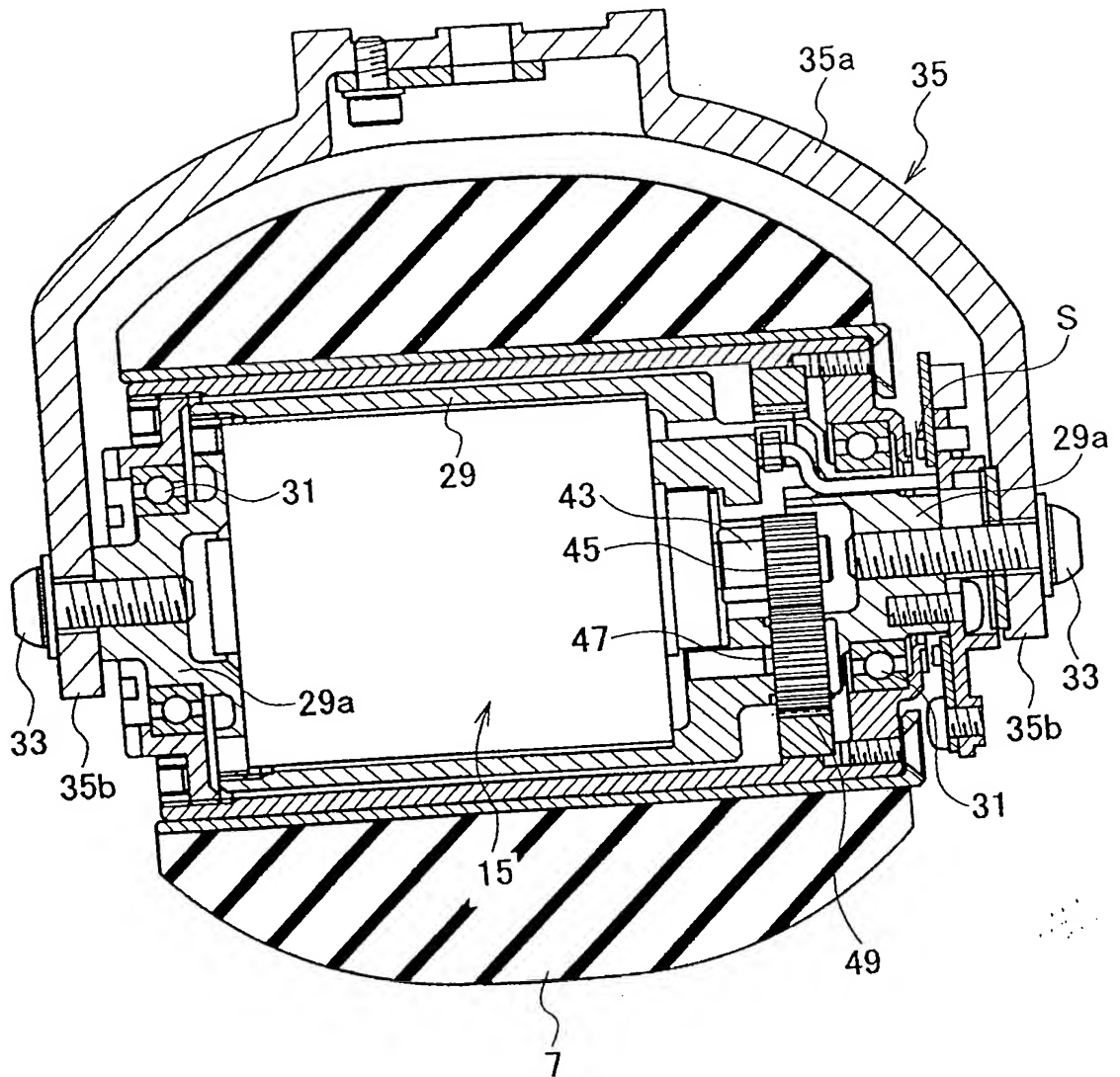


FIG. 3



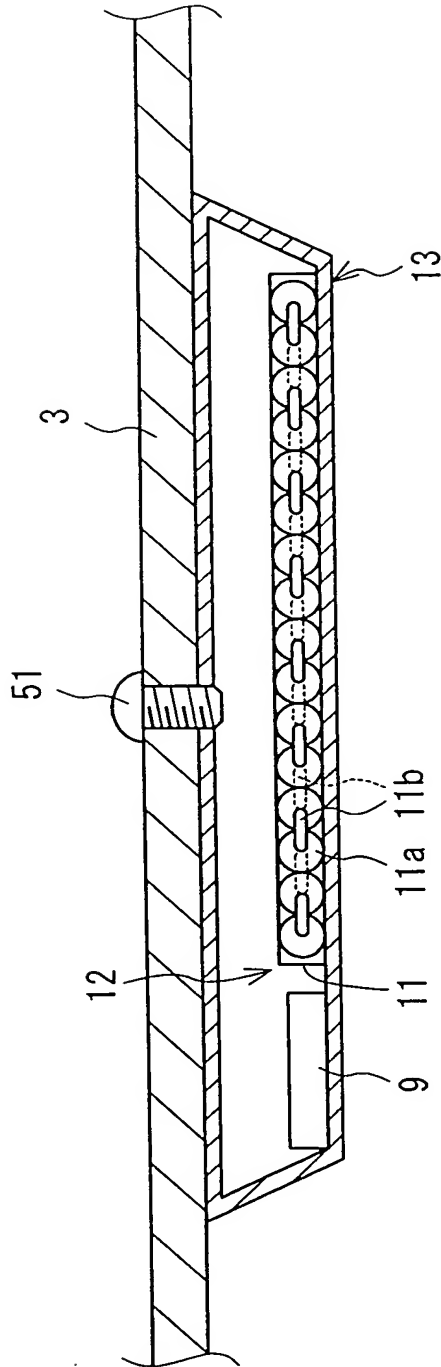
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FIG. 4



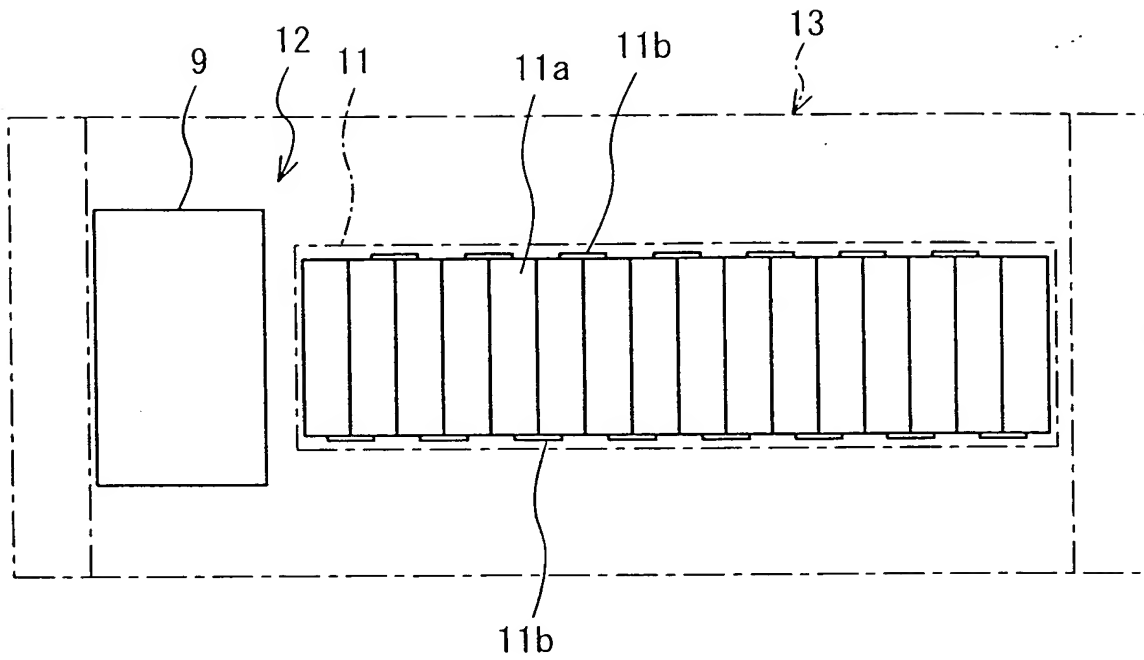
10/539240

FIG. 5



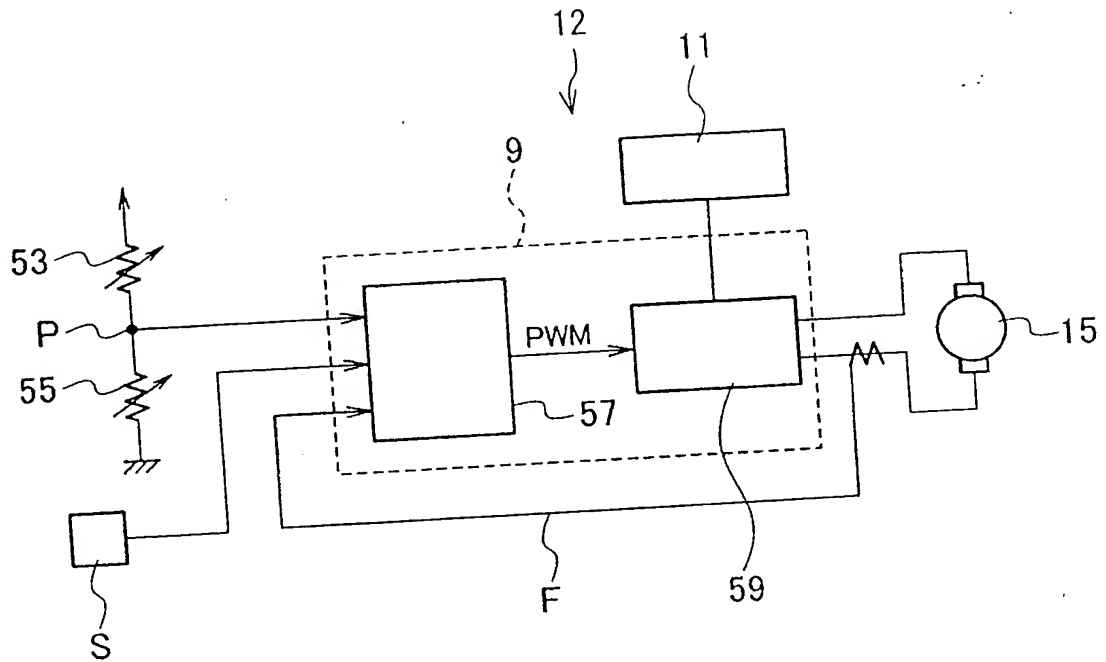
10/539240

FIG. 6



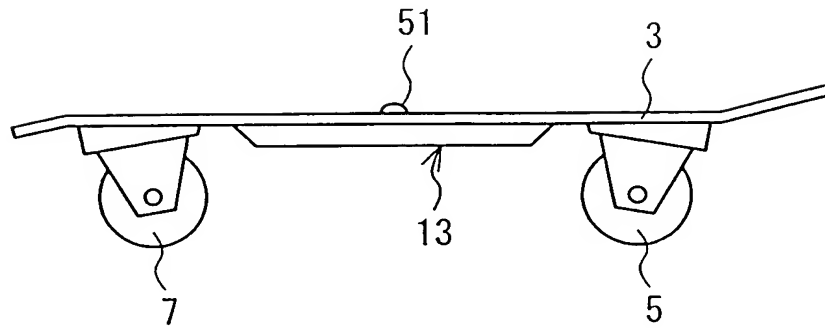
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FIG. 7.



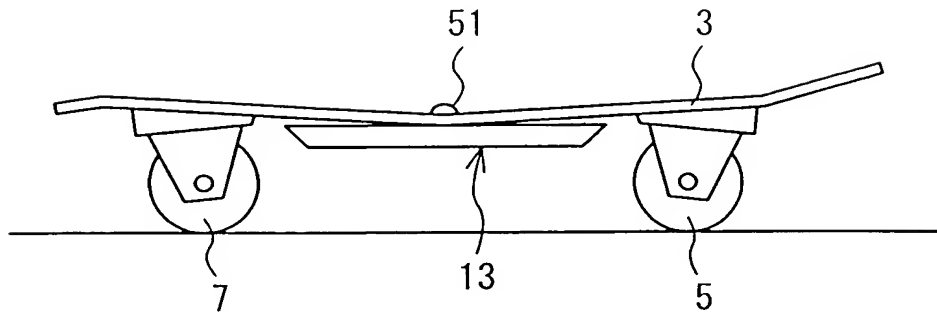
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FIG. 8



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FIG. 9



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FIG. 10 (a)

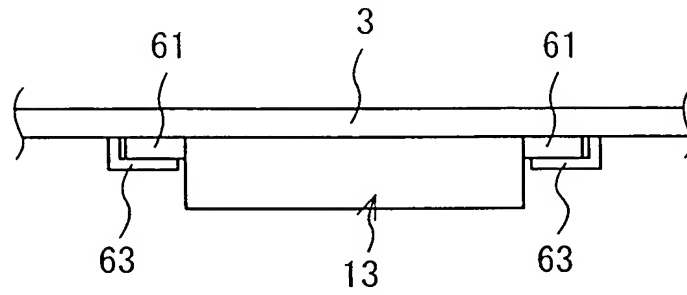
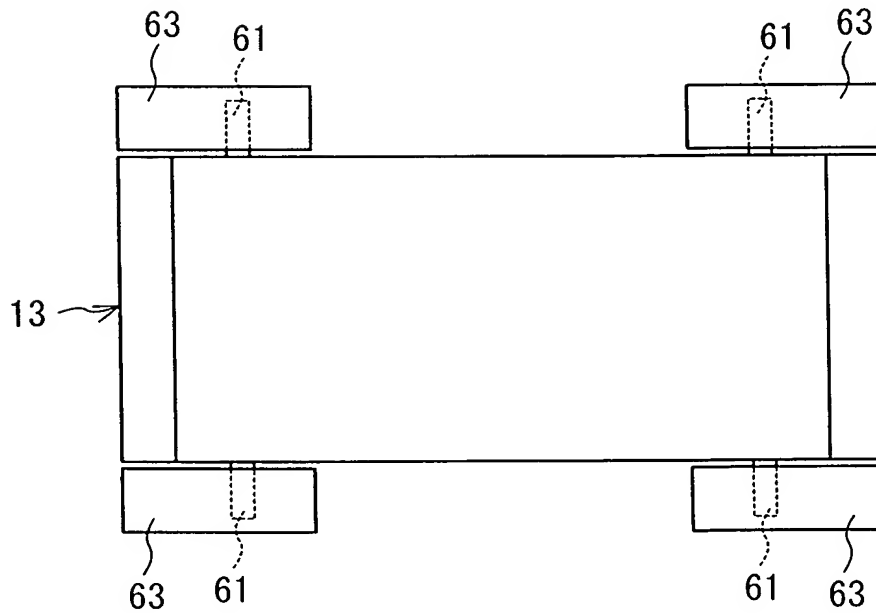
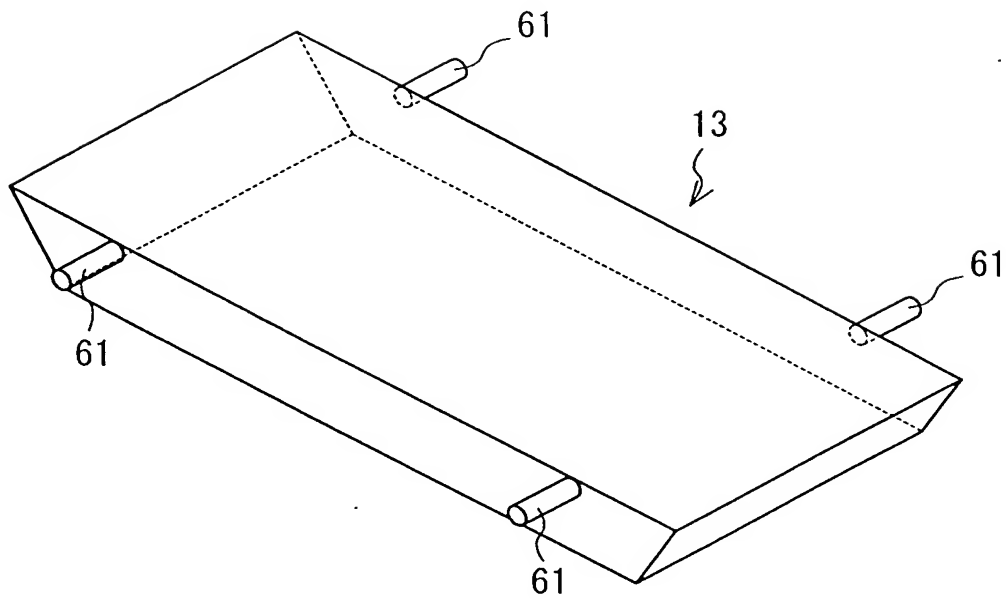


FIG. 10 (b)



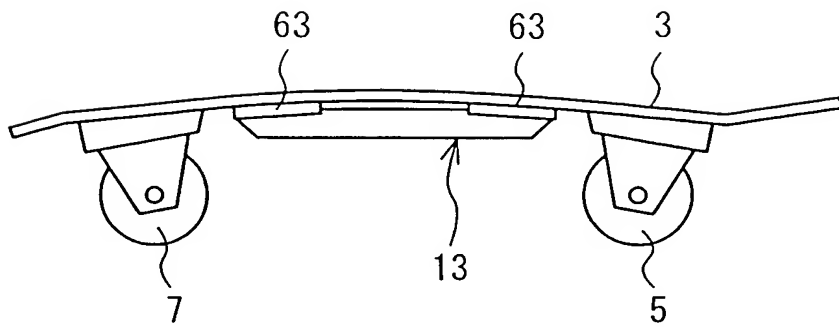
10/539240

FIG. 11



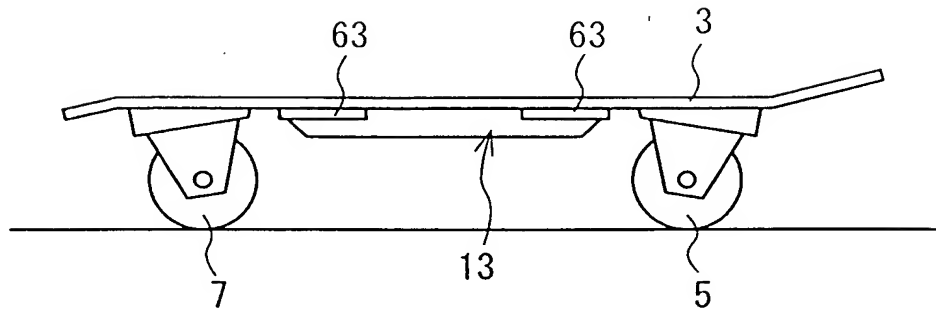
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FIG. 12



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FIG. 13



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FIG. 14 (a)

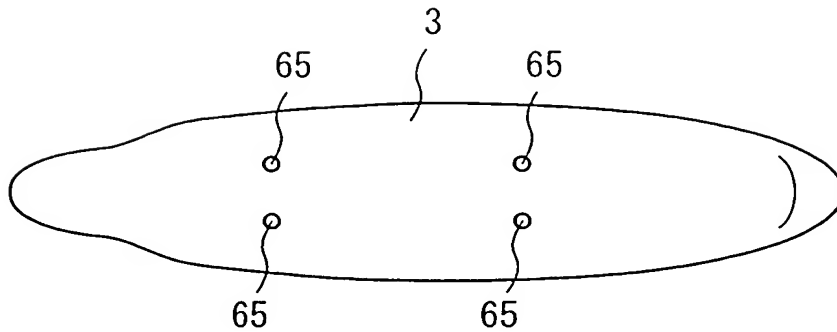


FIG. 14 (b)

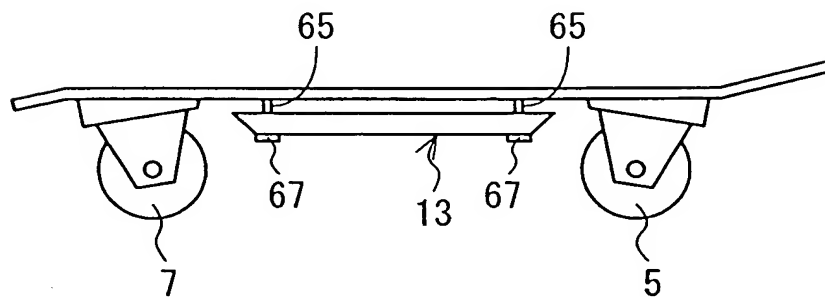
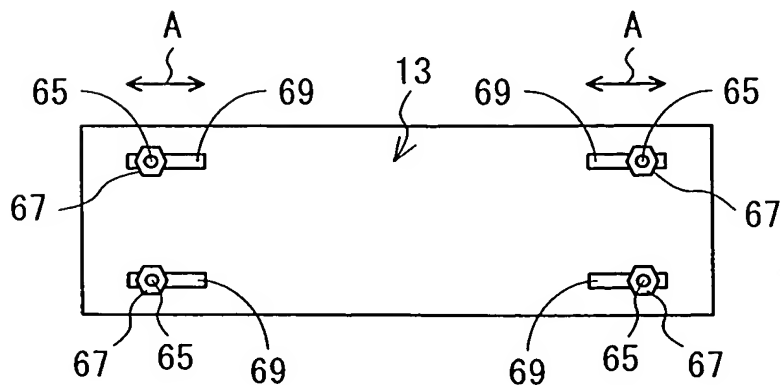


FIG. 14 (c)



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FIG. 15 (a)

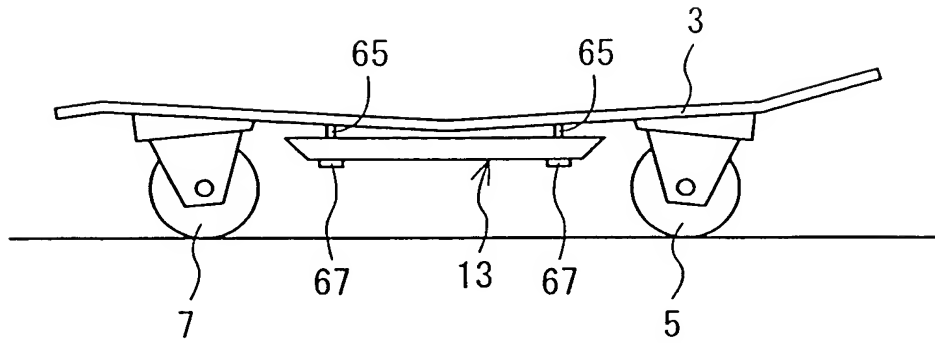


FIG. 15 (b)

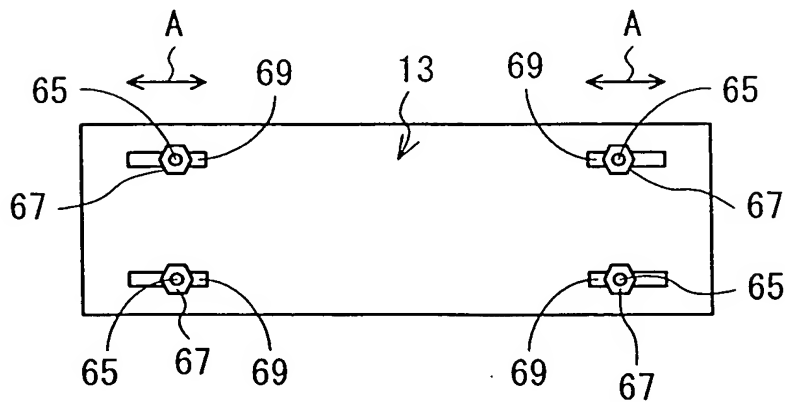


Fig. 1 is a cross-sectional view of a first embodiment of a semiconductor device. The device consists of a substrate 3. A top layer 12 is formed on the substrate 3. A central region of the top layer 12 contains a stack of layers. The stack includes a bottom layer 9a, a middle layer 11, and a top layer 13. The middle layer 11 has a patterned top surface with regions 11a and 11b. A screw 51 is shown securing the top layer 12.